CLAIMS

1. A transistor comprising:

a base well of a first conductivity type;

first, second and third conductive regions within the base well, having a second conductivity type and forming emitter and collector regions, one of said emitter and collector regions comprising an internal conductive region and an external conductive region, said external conductive region having an annular shape and said internal conductive region extending internally and at a distance from said external conductive region, and in that another of said emitter and collector regions comprises an intermediate conductive region, of an annular shape, extending between and at a distance from said internal and external conductive regions.

2. The transistor according to claim 1 wherein said internal, intermediate and external conductive regions are concentric to each other.

3. The transistor according to claim 1 wherein said internal conductive region is of solid shape.

4. The transistor according to claim 1 wherein said internal conductive region has a substantially circular shape, said intermediate conductive region has a substantially annular shape, and said external conductive region has an internal perimeter with a substantially circumferential shape.

5. The transistor according to claim 1 wherein said internal conductive region and said external conductive region are electrically connected by a metal region extending on top of said base well.

6. The transistor according to claim 1, further comprising: an internal metal region, overlying and in electrical contact with said internal conductive region; an intermediate metal region, of open shape, overlying and in electrical contact with said intermediate conductive region, said intermediate metal region having two facing ends set at a distance apart from one another; an external metal region, overlying and in electrical contact with said external conductive region; and a metal connection region, connecting said internal metal region to said external metal region and extending between said ends of said intermediate metal region.

7. The transistor according to claim 6 wherein said internal, intermediate, external and connection metal regions extend on a same level.

8. The transistor according to claim 1 wherein said internal and external conductive regions are collector regions and said intermediate region is an emitter region.

9. The transistor according to claim 1, forming a transistor of PNP type.

10. The transistor according to claim 1 forming a transistor of NPN type.

11. A semiconductor device comprising:

a base well of a first conductivity type;

an outer conductive region of a second conductive type formed within the base well, having a substantially annular shape, said outer conductive region being connected to a first metal contact;

an intermediate conductive region of the second conductive type formed within the outer conductive region, extending therefrom at a first distance and having a

substantially annular shape, said intermediate conductive region being connected to a second metal contact; and

an inner conductive region of the second conductive type formed within the intermediate conductive region, extending therefrom at a second distance, having a substantially circular shape, said inner conductive region being connected to a third metal contact.

12. The semiconductor of claim 11 further comprising a common metal contact region connecting the first and the third metal contacts.

13. The semiconductor of claim 12 wherein the inner and outer conductive regions forming an first electrode of a transistor, the intermediate conductive region forming a second electrode of the transistor, and the base well forming the base of the transistor.

14. The semiconductor of claim 13 wherein the first electrode is the collector of the transistor, and the second electrode is the emitter of the transistor.

15. The semiconductor of claim 11 wherein:

the outer conductive region is a first electrode of a first transistor;

the intermediate conductive region is simultaneously a second electrode of the first transistor and a first electrode of a second transistor;

the inner conductive region is a second electrode of the second transistor; and

the base well is a common base for the first and second transistor.

16. A semiconductor device comprising:

a base well of a first conductivity type;

a first conductive region of a second conductivity type having a substantially annular shape and being connected to a first metal contact, said first conductive region having an inner wall and outer wall;

a second conductive region of the second conductive type having a substantially annular shape and being connected to a second metal contact, said second conductive region being positioned at a first distance from the inner wall of the first conductive region; and

a third conductive region of the second conductive type having a substantially circular shape and being connected to a third metal contact, said third conductive region being positioned at a second distance, greater than the first distance, from the inner wall of the first conductive region.

17. The semiconductor device of claim 16 wherein the first and third conductive regions are two different input terminals to two different transistors.

18. The semiconductor device of claim 16 wherein the first and third conductive regions are electrically coupled together and are a common input terminal to a single transistor.

19. A semiconductor device comprising:

a base well of a first conductivity type;

a first conductive region of a second conductive type formed within the base well, having a substantially annular shape, said first conductive region being connected to a first metal contact;

a second conductive region of the second conductive type formed adjacent to the first conductive region, spaced therefrom a first distance and having a substantially annular shape and being positioned on a first side of the first conductive region, said second conductive region being connected to a second metal contact; and

a third conductive region of the second conductive type formed adjacent to the second conductive region, spaced therefrom a second distance, having a substantially circular shape and being positioned on the first side of the first conductive region, said third conductive region being connected to a third metal contact.

20. A process for fabricating a semiconductor device, comprising:

forming a base well with a first conductivity type; and

forming outer, intermediate and inner conductive regions with a second conductivity type within the base well in a substantially concentric manner, the outer and intermediate conductive regions each being a substantially annular shape, and the inner conductive region being a substantially circular shape.

21. The process of claim 20 further comprising connecting the inner and outer conductive region by a common metal contact.

22. The process of claim 20 further comprising independently connecting the inner and outer conductive regions to two separate metal regions.

23. A method comprising:

applying a first voltage potential to a base of a transistor, the base being formed by a base well of a first conductivity type;

applying a second voltage potential to a first electrode of a transistor, the first electrode being an outer and inner conductive regions of a second conductivity type formed in the base well in a substantially concentric manner and connected to a common metal region; and

applying a third voltage potential to a second electrode of a transistor, the second electrode being an intermediate conductive region of the second conductivity type formed in the base well in a substantially concentric manner with respect to the inner conductive region.

24. The method of claim 23 wherein the first electrode is a collector of the transistor, the second electrode is an emitter of the transistor.

25. A method comprising:

applying a first voltage potential to the base of a first transistor, said base being formed by a base well of a first conductivity type;

applying a second voltage potential to a first electrode of the first transistor, said electrode being connected to an inner conductive region of a second conductivity type, having a substantially circular shape formed within the base well;

applying a third voltage potential to a second electrode of the first transistor, said electrode being connected to an intermediate conductive region of a second conductivity type, having a substantially annular shape and surrounding the inner conductive region in a concentric manner, thereby obtaining a first current gain;

applying a forth voltage potential to the base of a second transistor, said base being formed by the same base well of the first transistor;

applying a fifth voltage potential to a first electrode of the second transistor, said electrode being connected to an outer conductive region of a second conductive type, having a substantially annular shape and surrounding the intermediate conductive region in a concentric manner; and

applying a sixth voltage potential to a second electrode of the second transistor, said electrode being connected to the intermediate conductive region, thereby obtaining a second current gain.

26. The method of claim 25 wherein the first electrode of the first transistor is a collector, the second electrode of the first transistor is an emitter, the first electrode of the second transistor is a collector, and the second electrode of the second transistor is an emitter.